Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A LC-Display with n gate driver and source drivers for driving the LC-Display with dots arranged in x rows and y columns, wherein the gate drivers ~~comprises~~ comprise several output stages for driving the gate lines of the LC-Display, the LC-Display comprising:

a gate on supply line VH to turn on a transistor of the LC-Display;

a gate off supply line VL to turn off a transistor of the LC-Display, wherein the gate off supply line VL;

an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL; and

a circuit to connect a storage capacitance Cst of a selected gate line GLy to the additional gate off supply line VLclean and to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL.

2. (previously presented) The LC-Display as claimed in claim 1, wherein the output stage comprises:

a PMOS transistor MP1 arranged between the gate on supply line VH and an output of the output stage;

a first NMOS transistor MN1 arranged between the gate off supply line VL and the output of the output stage; and

a second NMOS transistor MN2 arranged between the additional gate off supply line VLclean and the output of the output stage.

3. (previously presented) The LC-Display as claimed in claim 1, wherein the additional gate off supply line VLclean is routed over a separate track on the LC-Display glass.

4. (previously presented) The LC-Display as claimed in claim 1, wherein a track of the gate off supply line VL and a track of the additional supply line VLclean are coupled to a same supply level.

5. (previously presented) The LC-Display as claimed in claim 1, further comprising a power supply to supply a voltage to the gate off supply line VL and the additional gate off supply line VLclean, wherein a track of the gate off supply line VL and a track of the additional gate off supply line VLclean are connected together in a location where a track impedance to an output of the power supply is relatively low.

6. (previously presented) A method for driving a display with n gate drivers and at least one source driver, the method comprising:

arranging dots in x rows and y columns;

providing several output stages for driving gate lines of the display;

providing a gate on supply line VH to turn on a transistor of the LC-Display;

providing a gate off supply line VL to turn off a transistor of the LC-Display;

providing an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL;

connecting a capacitance of a selected gate line to a previous gate line; and

activating an additional supply line VLclean of the output stage for the selected gate line with the supply line VL when the previous gate line is activated.

7. (previously presented) A method for driving a display with n gate drivers and a source driver, the method comprising:

arranging dots in x rows and y columns;

providing several output stages for driving gate lines of the display;

providing a gate on supply line VH to turn on a transistor of the LC-Display;

providing a gate off supply line VL to turn off a transistor of the LC-Display;

providing an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL;

connecting a capacitance of a selected gate line to a next gate line; and

activating an additional supply line VLclean of the output stage for the selected gate line with the supply line VL when the next gate line is activated.